# Anisotropic mobility in large grain size solution processed organic semiconductor thin films

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The hollow pen method for writing thin films of materials from solution is utilized to deposit films of 6,13-bis(tri-isopropylsilylethynyl) pentacene (TIPS pentacene) onto $SiO_2$ surfaces with pre-patterned source/drain gold contacts. We demonstrate that large domains are obtained for TIPS pentacene films deposited from 0.5–4.0 wt % solutions with toluene. Crystalline grains with (001) orientation are observed to grow with sizes that can exceed 1 mm along the writing direction. A preferred azimuthal orientation is also selected by the process, resulting in anisotropic field effect transistor mobility in the films. © *2008 American Institute of Physics*. [DOI: 10.1063/1.2839394]

Organic semiconductors have recently attracted significant interest as materials for applications in low-cost or large-area microelectronics. For example, displays based on organic light emitting diodes have reached an advanced stage of development.[1] Additional applications such as display drivers, radio frequency identification tags, and sensors are also rapidly progressing.[2]

New materials and processing methods for solution deposited films are currently needed in order to drive further research in this area. In particular, direct-write methods with high linear velocity have the potential to be scaled up into roll-to-roll processes. A long-standing goal of organic electronics is to achieve a crystalline grain size larger than the channel length of typical organic field-effect transistors (OFETs). Ideally, high throughput and high performance will be obtained simultaneously, although there will be trade-offs between processing speed and material properties such as grain size, defect density, and carrier mobility.

Here, we demonstrate that large grain sizes can be obtained by solution processing and describe the effect of large grain size on the field-effect mobility in OFETs. We have used the hollow pen method to deposit thin films of 6,13-bis(tri-isopropysilylethynyl) pentacene (TIPS pentacene). TIPS pentacene is a promising material because, unlike unsubstituted pentacene, it is highly soluble in common organic solvents. The face-to-face packing of TIPS pentacene in crystalline form is optimal for $\pi$-orbital overlap, leading to a relatively high but directionally anisotropic carrier mobility.[3–6]

The deposition technique used in this study is a direct-write method using a hollow pen consisting of a 1.0 mm borosilicate glass capillary. A solution with a concentration of 0.5–4.0 wt % in toluene is held in the pen by capillary forces. Film deposition is accomplished by allowing the microdroplet of solution on the end of the pen to make contact with the surface and then laterally translating the pen at a controlled rate, typically 0.1–4.0 cm/min. This very simple process produces a highly ordered thin layer of material, typically with a thickness between 100 and 300 nm, with the width of the deposited film line determined by the pen diameter. The process has advantages similar to the dip-coating method, such as large crystalline grain size,[7] but it is more controllable and more amenable to scaling up for large-area deposition. The method also has advantages relative to ink-jet printing, since it produces fully continuous films, while, in contrast, pixellation can degrade film properties of ink-jet printed layers.

Transistors are fabricated by the following procedure: A heavily doped *p*-type Si substrate with a 300 nm thermally grown $SiO_2$ layer is degreased in acetone and methanol. Gold is evaporated through a shadow mask to form source and drain electrodes with a 75 $\mu$m channel length. The semiconductor layer is deposited atop the gold/$SiO_2$, creating a "bottom-contact" transistor geometry in which the source and drain are beneath the semiconductor layer, and the substrate serves as the gate contact. Single transistors and arrays of four-channel transistor groups consisting of four source/drain electrodes are fabricated. As illustrated in Fig. 1(a), the four-channel geometry contains top and bottom branches that are oriented so that the carriers traverse the channel in the *x* direction, while the left and right branches are oriented to test the mobility in the *y* direction.

Structural characterization is performed by optical microscopy using a microscope equipped with rotatable linear polarizers and a rotatable sample stage. Bright-field and polarization mode images are recorded for each transistor channel. Figure 1(b) shows a polarization mode image of a single OFET with a 75 $\mu$m by 1.0 mm channel, visible as a dark line near the center of the image. The TIPS pentacene line was deposited from the top left toward the lower right using a 0.5 wt % solution at a speed of 1.3 cm/min. Crystalline grains are observed to extend from the edges of the line inward at an angle inclined toward the writing direction. Large grains near the center of the line are more closely aligned to the writing direction. Small dark regions are observed on some grains due to thickness variations. We note that the grain size observed, which can exceed 1 mm along the writing direction, is significantly larger than that obtained by other deposition methods.[6]

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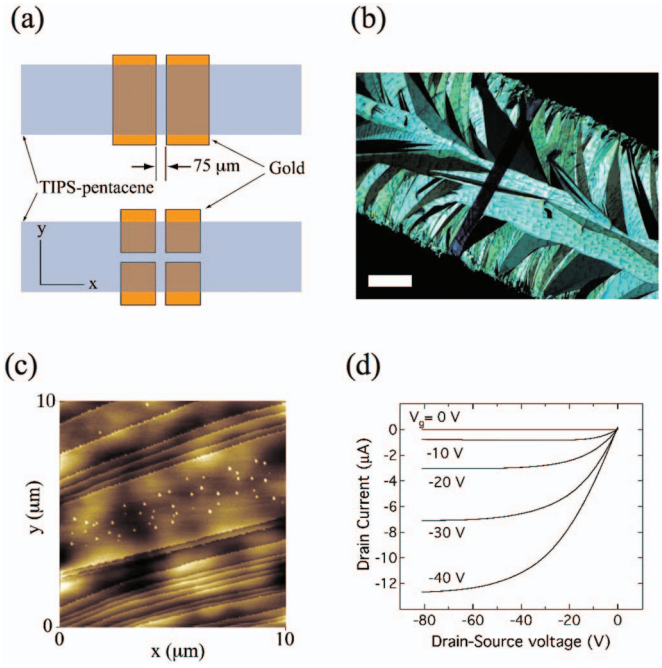


FIG. 1. (Color) (a) TIPS pentacene lines are deposited over source and drain contacts using a 1.0 mm pen. Both single transistor and four-channel contact geometries are depicted. (b) A polarization mode optical micrograph shows crystalline grains bridging across the transistor channel. The scale bar represents 250 $\mu$m. (c) Atomic force microscopy image showing the surface structure of a TIPS pentacene film. Molecular height steps and small islands on the wider terraces are readily visible. (d) Current-voltage characteristics of the transistor shown in (b).

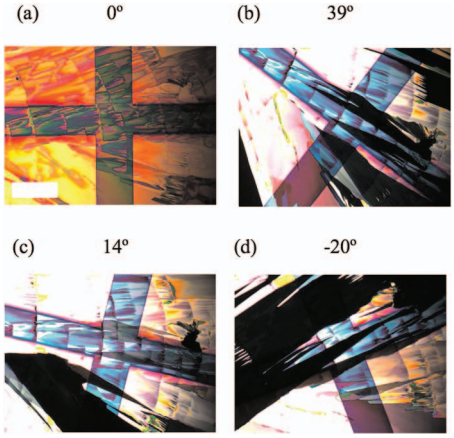


FIG. 2. (Color) (a) Bright-field optical micrograph of a film deposited over four gold contacts. The writing direction was from right to left in the image, the concentration was 4 wt %, and the writing speed was 0.48 cm/min. The four-transistor channels thus formed have dimensions of $75 \times 500$ $\mu$m$^2$. Variations in the color of the film within the channel region are from film thickness variation. The scale bar represents 100 $\mu$m. [(b)–(d)] Polarization mode micrographs in three sample orientations. The orientations relative to (a) are displayed above each image. The three images are complementary, and the dark grains collectively account for >95% of the imaged area.

Atomic force microscopy images have also been obtained for selected samples. Figure 1(c) shows an image obtained in tapping mode, with a total vertical range of 7.6 nm. The image is from the channel region of a film deposited from a 2 wt % solution at a speed of 0.3 cm/min. Molecular steps are visible, forming uniform terraces with a step height of ~2 nm. This is comparable to the layer spacing derived from the crystal structure. Since the *c* axis is at a small angle to the surface normal, the layer spacing is 1.65 nm. These results show that the material within a single grain is crystalline.

Current-voltage curves at varying gate bias are measured using a probe station to contact the source and drain electrodes in air. Figure 1(d) shows a set of *I-V* curves for the same transistor shown in Fig. 1(b). A field effect mobility of $\mu$=0.09 cm$^2$/V s is extracted from the data. We have performed many measurements on additional transistors and have observed mobility values ranging up to 0.14 cm$^2$/V s, with a clear dependence on crystalline grain size.

In this letter, we would like to also demonstrate the link between carrier mobility and structure. Therefore, we have chosen to fabricate arrays of transistors in clusters of four electrodes close together, as illustrated in Fig. 1(a). This geometry allows two types of observations: (i) The correlation in mobility values for neighboring transistors in the same orientation can be analyzed in order to distinguish variations due to grain structure from variations due to locally uncontrolled effects. (ii) Since the carrier mobility in TIPS pentacene is directional,[5] it is important to also study the distribution of grain orientations in transistor structures. The four-transistor geometry allows us to independently extract the local mobility in two orthogonal directions: along the writing direction of a semiconductor line and perpendicular to it.

Figure 2 shows a study of the grain orientation for a film deposited over four gold contacts in the four-channel geometry, which is one of an array of 40 similar structures. Figure 2(a) shows a bright-field image, where the channel regions of the four-transistors are clearly visible. The measured mobility values for the four-transistor channels are (bottom) 0.06, (top) 0.045, (right) 0.004, and (left) 0.006, all in units of cm$^2$/V s. Note the striking order-of-magnitude disparity between the top/bottom versus the left/right values. Below, we will refer to the top, bottom, left, and right channels as *T*, *B*, *L*, and *R*, respectively.

Figure 2(d) shows that a single large grain bridges across both the *L* and *T* transistor channels; nevertheless, they exhibit mobility values that differ by a factor of 7.5. This difference appears to be predominantly due to mobility anisotropy. On the other hand, Figs. 2(b) and 2(d) together show that the *R* channel has a larger density of grain boundaries, which are oriented so that carriers must encounter several of them while traversing the channel. Therefore, it make sense that the *R* channel exhibits the lowest mobility of the four. In addition, we speculate that the dark grain oriented at 14° in Fig. 2(c) is close to the optimum orientation for carriers traversing in the *x* direction, leading to the higher mobility observed for the *B* channel. This conjecture is based on a partial determination of the crystallographic orientation of the grain, which we will explain below.

In order to gain information about the grain orientation, a single crystal of TIPS pentacene with a known crystallographic orientation was also examined by polarization microscopy. The *c** face of the crystal was adjusted to the extinction orientation in the *a*-*b* plane, thereby determining that extinction occurs when the angle between the crystal *a* axis and the polarizer is $\phi_{ext}$=−32°, where the (negative) direction is away from the *b* axis. For comparison, we note that Ostroverkhova *et al.* have found that the highest mobility orientation occurs at $\phi_1$=−14°.[5] Combining these observations, we infer an 18° orientation difference between extinction in polarization microscopy and the direction of highest

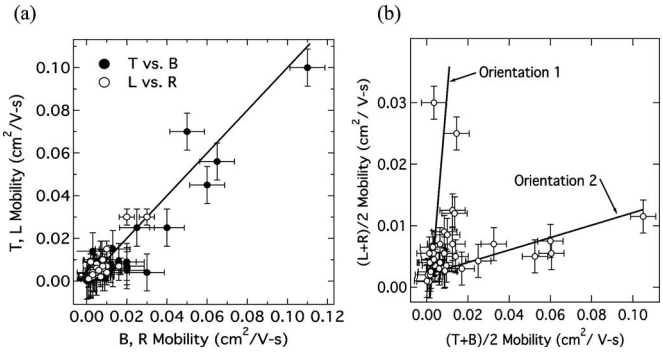


FIG. 3. Mobility data extracted from $I_{DS}$ vs $V_g$ curves for an array of 40 four-transistor structures. (a) Correlations for transistors in the same orientation. (b) Correlations for transistors in orthogonal orientations. The lines labeled orientation 1 and orientation 2 are for the model with two preferred grain orientations, which is described in the main text.

intrinsic hole mobility. Therefore, it is plausible that the large grain at 14° in Fig. 2(c) is very close to the optimum orientation (18°) relative to the transistor channel. However, we also note that there is a 90° ambiguity inherent in polarization microscopy, preventing an unambiguous assignment of grain orientation from microscopy alone.

We now turn to a discussion of transistor mobility correlations. A $40\times4$ array of transistors is prepared at writing speeds between 0.08 and 1.3 cm/min. The mobility results show that there is a large variation in the mobility even at a given speed. This is consistent with a variation in the grain size and grain orientation, which is also observed by visual inspection of the films. A remarkable feature of the data is that, although there is considerable variation in the measured values, the measurements within the same transistor structure and in the same orientation tend to be very close. A correlation plot of the mobility data for transistors in the same orientation is shown in Fig. 3(a), illustrating this effect. Linear correlations coefficients are $r=0.95$ for the $T$ vs $B$ data and $r=0.85$ for the $L$ vs $R$ data. This high degree of correlation is meaningful because it shows that random measurement errors are small and that the large variations in the data are caused by effects occurring on a length scale larger than 1 mm. We have also performed similar measurements on transistors made from drop-cast films with grain sizes $<10$ $\mu$m and have found no evidence for high correlations, suggesting that the correlation effect only occurs for films with very large grain sizes.

The cross-correlation plot for transistors oriented 90° from each other is shown in Fig. 3(b), and it exhibits a very different pattern. Note that there are no examples of four-transistor structures that exhibit high mobility in *both* directions. Using error bars obtained from Fig. 3(a), we find that modeling the data as linearly correlated results in a very large $\chi^2$ parameter of 78.6 (it should be close to 1 for an acceptable fit). Since the probability of obtaining data that give this large $\chi^2$ value by chance is infinitesimally small, it is a statistical certainty that transistors in orthogonal orientations are *not* linearly correlated. The difference between Figs. 3(a) and 3(b) directly shows that film structure has an effect on mobility because other effects such as variations in interface quality would not produce such an anisotropy.

Instead, we suggest that the data in Fig. 3(b) are a result of the grain structure and the intrinsic anisotropy in the mobility. Following this conjecture, the data can be explained by a model consisting of just two orthogonal preferred orientations relative to the writing direction. Either one preferred range of grain orientations or the other is assumed to occur on each four-transistor structure, resulting in higher mobility in either the $x$ or the $y$ direction, as we observe. The best-fit lines, which correspond to a reduced $\chi^2$ of 0.41, are shown in Fig. 3(b). This simple two-orientation model is statistically significant at about a 99% level. We note that the lines labeled "Grain Orientation 1" and "Grain Orientation 2" have slopes of 4 and 1/10, which indicate the magnitude of the mobility anisotropy in the $a$-$b$ plane.

In this letter, we have established that there is a link between the structure and mobility in large grain size organic semiconductor thin films. The observed correlations show that the large range of mobility values measured for different transistors cannot be predominantly due to other effects, such as local variations in interface quality. However, this does not imply that interfaces are of no importance. Indeed, our future efforts will include optimization of field-effect transistor mobility using UV-ozone treatment and/or self-assembled monolayers to improve the electronic properties of the oxide-semiconductor interface.[6]

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