# Radios – The Wireless Interface

Part 1

muse

# Objectives

- Understand the performance requirements of each component in the RF block diagram. *Links to communications systems analysis*
- Understand the design and technology challenges for each component in the RF block diagram
- Describe implications on the radio hardware design due to various types of scaling, e.g. size, frequency, cost, power, data rate. *Links to wireless network design*

# Outline

- Overview and RF Block Diagram
- Filters
- Amplifiers
- Up/Down Conversion
- Oscillators and Synthesizers
- Modulation Basics
- Antennas
- Chip-Level Radios
- Integration and Packaging

# Overview & RF Block Diagram

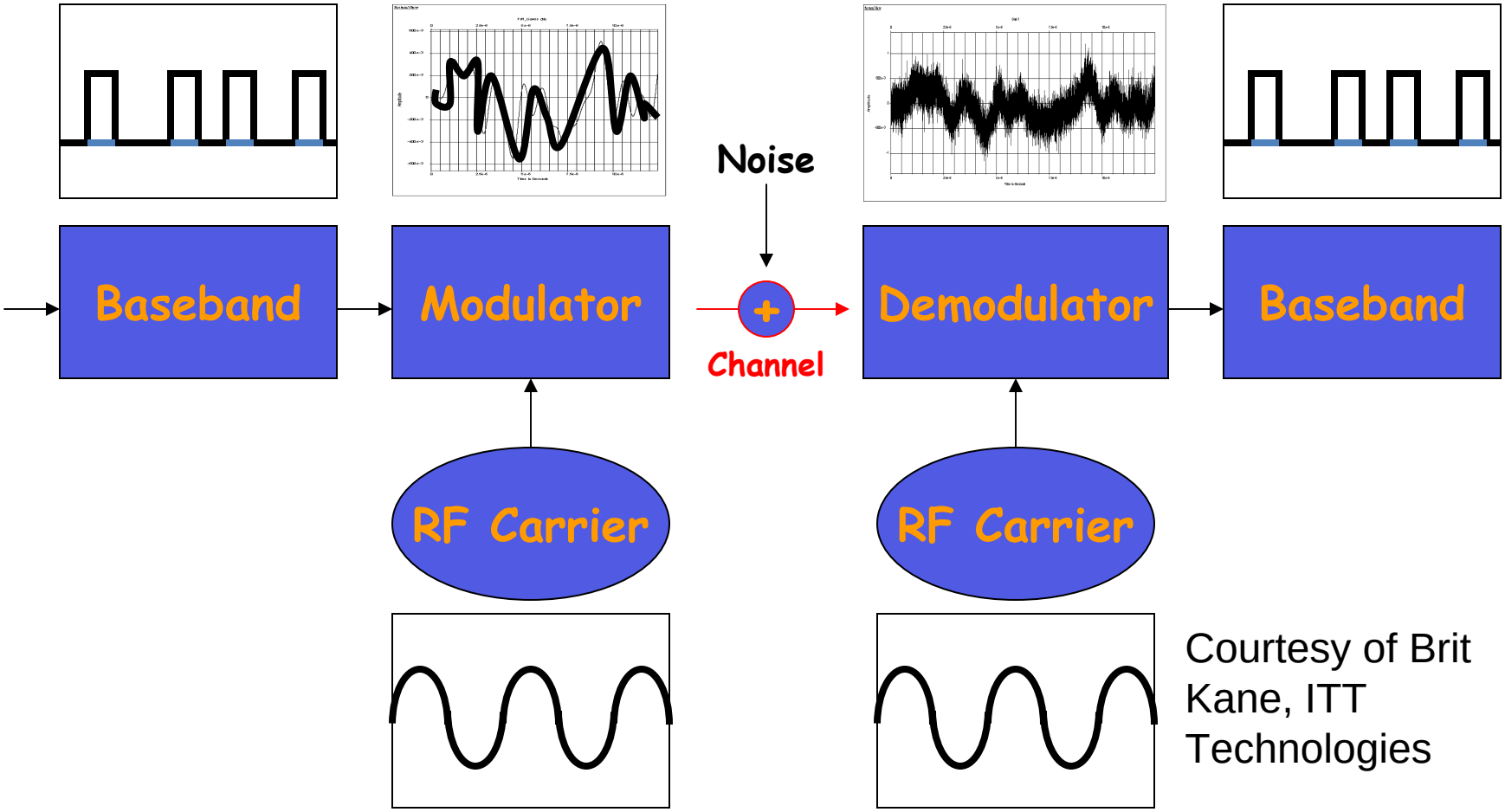
# Overview and RF Block Diagram

- Functional View of the Radio
- The Role of Analog RF Hardware in Today's Radios: RF Sub-system Block Diagrams & Requirements
- Some Design and Technology Issues
- Future Front-End Technology

# Functional View of the Radio

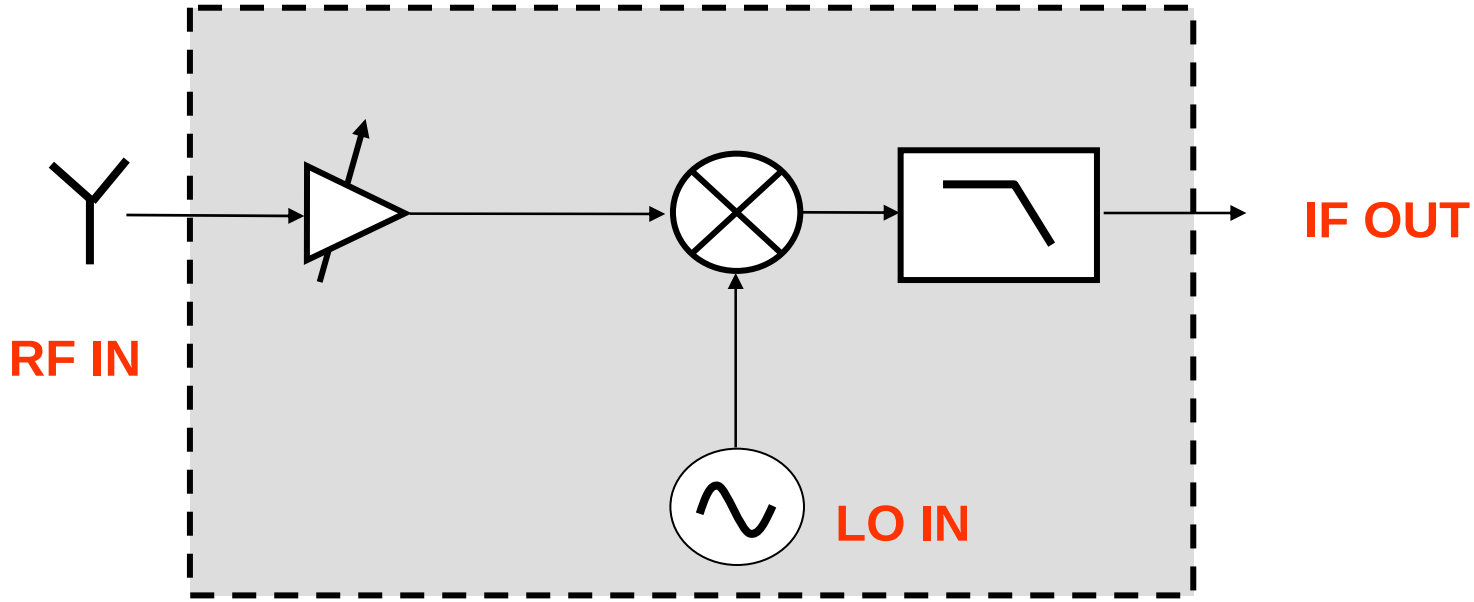
- Analog RF hardware – the link between the information (data) and the channel
- Multiple perspectives
  - High Level → how information is processed
  - Mid Level → components needed for each processing step
  - Low Level → design of each component

# RF Analog Block Diagram
# Information Processing




Courtesy of Brit Kane, ITT Technologies

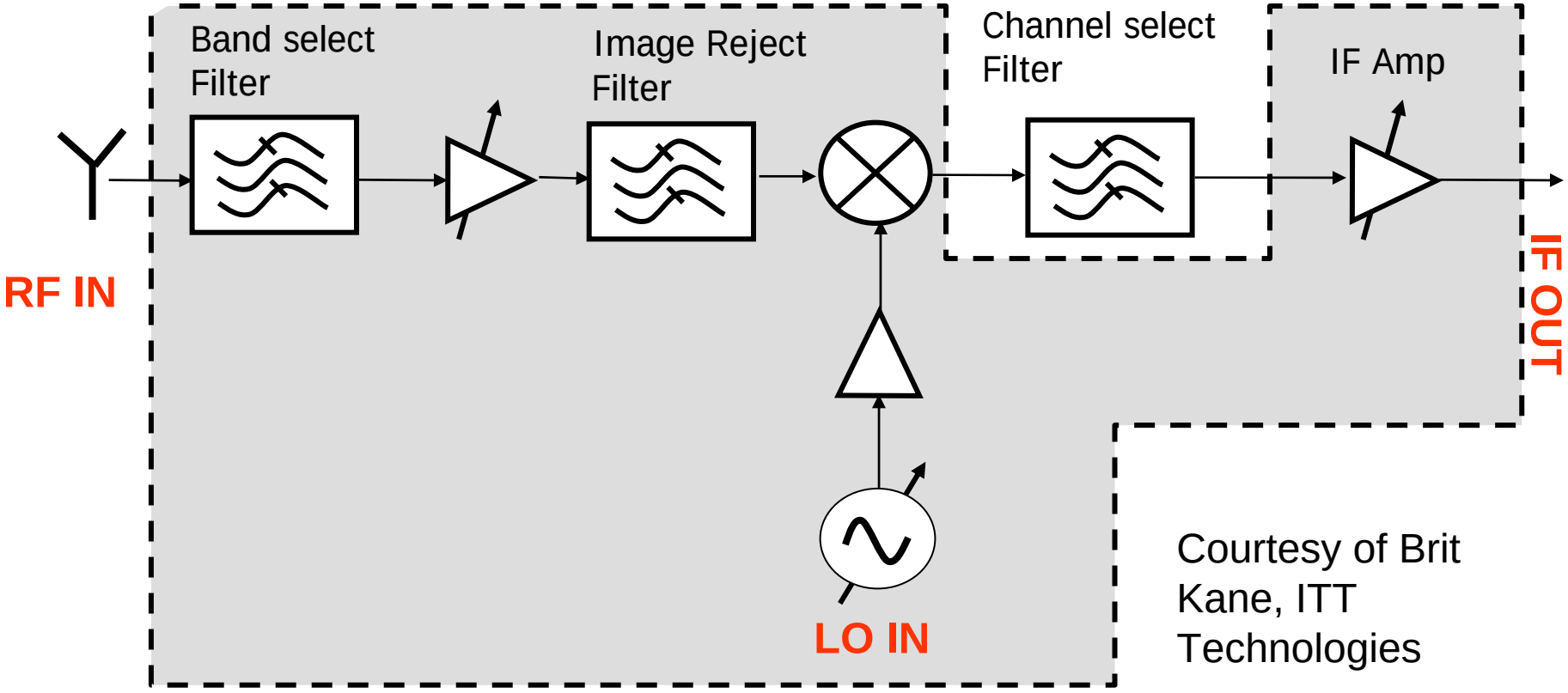
# RF Analog Block Diagram - Receiver



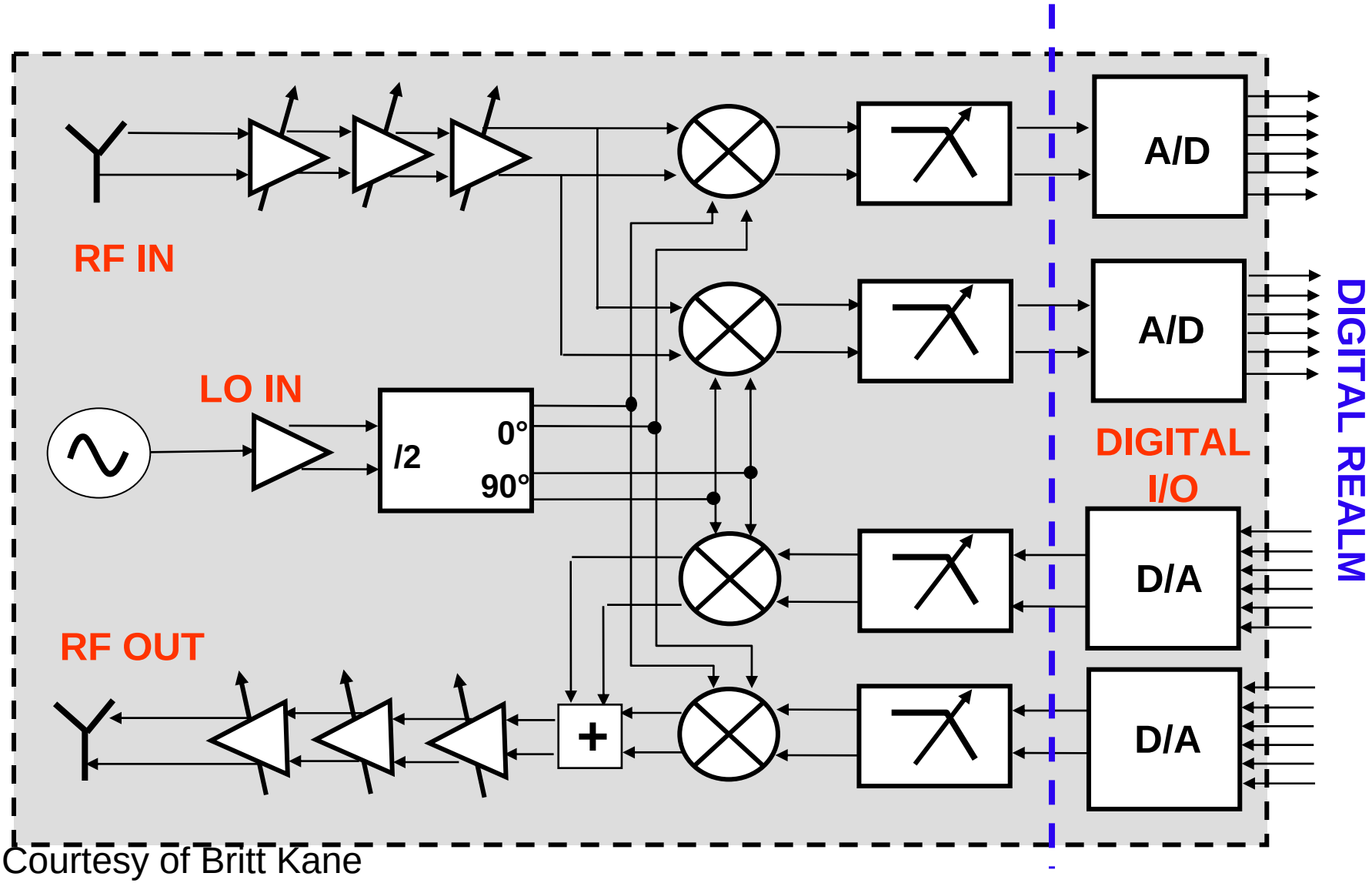


Courtesy of Britt Kane

# RF Analog Block Diagram - Receiver



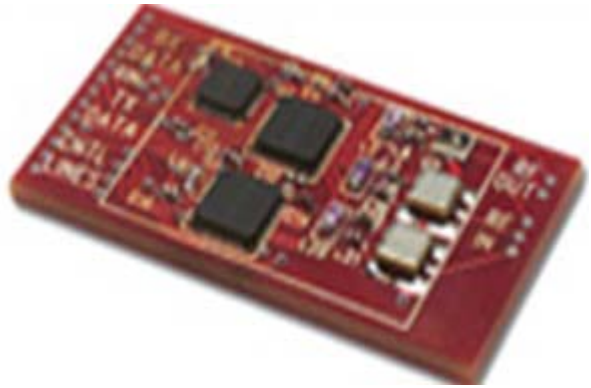
# RF Analog Block Diagram



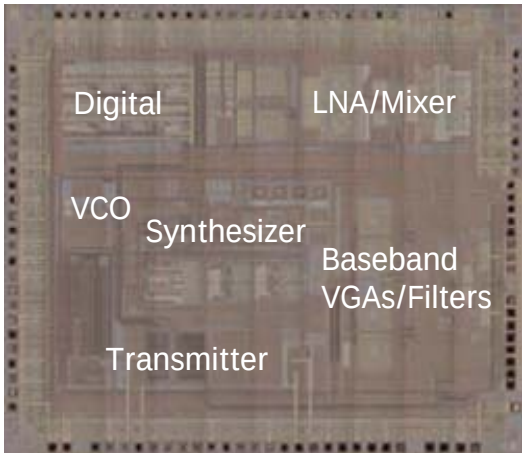

Courtesy of Britt Kane

# Some Design & Technology Issues

- Form: Board Level vs. Chip Level

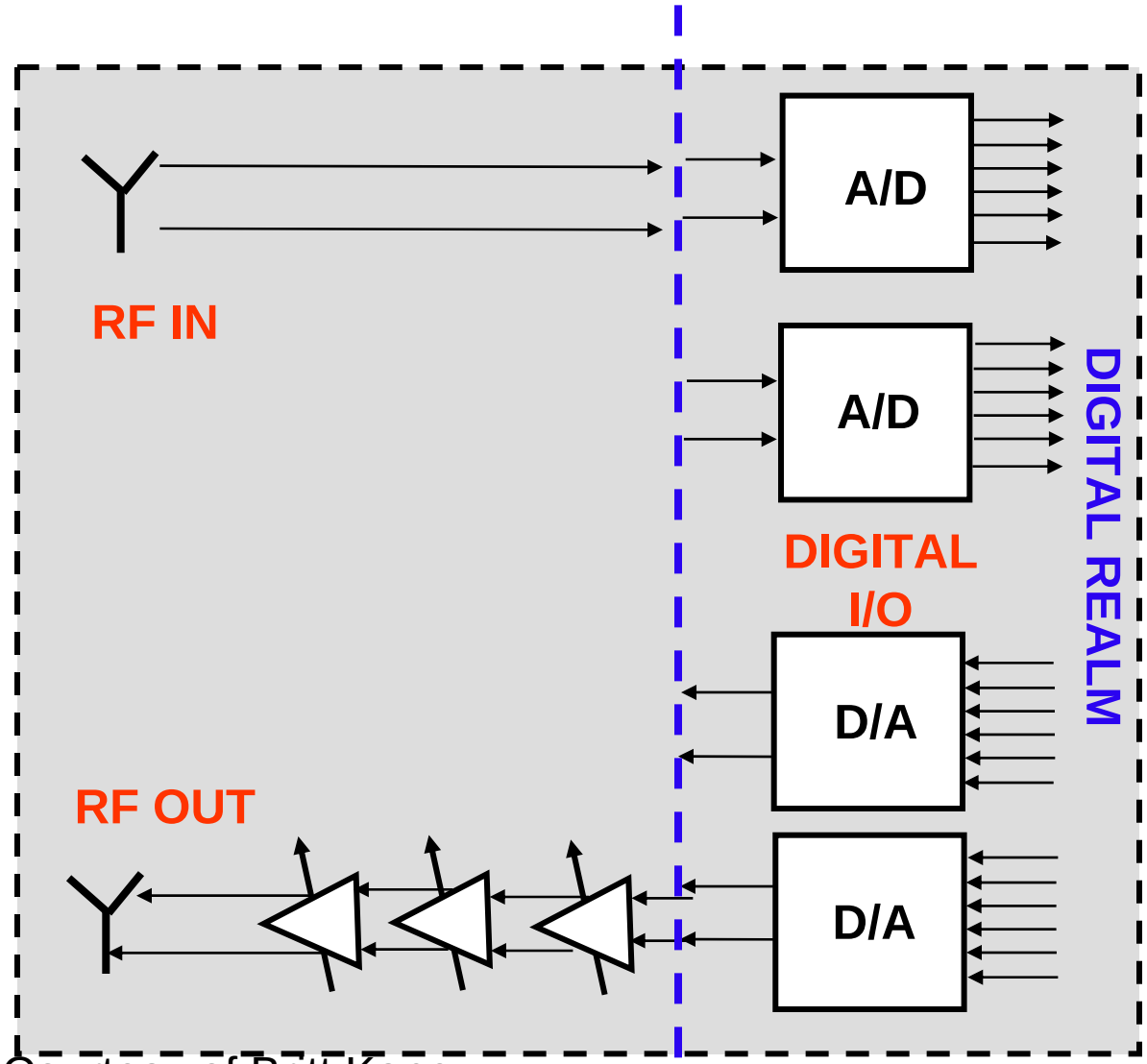


Not to scale!




- Architecture:
  - Down-conversion: Single vs. Dual vs. Zero
  - Dual-band, multi-band
  - Multi-channel, redundancy

# Future Front-End Technology




Courtesy of Britt Kane

# Overview – Conclusions

- RF analog hardware is the pathway between the data and the propagation channel
- Functional and then component-level block diagrams are the starting points for radio design
- The radio architecture defines how functional requirements flow down to the component / device level